# Introducing Atmel AT17LV Series FPGA Configuration Memories

## Features

- **EE Reprogrammable Serial Memories, Designed to Store Configuration Data for Field Programmable Devices**
- **Memory Sizes Include 65K, 128K, 256K, 512K, 1M, 2M and 4M Bits**
- **In-System Programmable via 2-wire Bus**
- **Simple Interface to SRAM FPGAs**
- **Programmable Reset Polarity**
- **High-reliability**
  - **Endurance: 100,000 Write Cycles**
  - **Data Retention: 90 Years for Industrial Parts (at 85°C) and 190 Years for Commercial Parts (at 70°C)**

## Introduction

The AT17LV series FPGA Configuration EEPROMs (Configurators) provide an easy-to-use, cost-effective configuration memory for Field Programmable Gate Arrays. Atmel configurators can also be used as memory storage devices for Field Programmable System Level Integrated Circuit (FPSLIC™) and other Digital Signal Processing (DSP) or programmable chips with a similar clock and data interface. The AT17LV series configurators use a simple serial-access procedure to configure one or more FPGA devices. The user can select the polarity of the reset function by programming four EEPROM bytes. These devices also support a write-protection mechanism within its programming mode.

The AT17LV series configurators can be programmed with industry-standard programming systems, Atmel ATDH2200E Programming Kit or Atmel ATDH2225 ISP Cable.

This application note explains the following topics:

- Selecting the EEPROM Density
- AT17LVxxx and AT17LVxxxA Configurators
- Selecting the Package Type
- Determining the Ordering Code
- Reading the Device Markings
- Programming Options
  - Drop-In/Standalone Programming
  - In-System Programming
- Programming File Formats
- Troubleshooting Hints

**AT17LV Series FPGA Configuration Memory**

**Application Note**

2295B-CNFG–09/02

## Selecting the EEPROM Density

Atmel AT17LV series EEPROMs are offered in 65K, 128K, 256K, 512K, 1M, 2M and 4M bits.

For Atmel FPGA or FPSLIC devices, select the density of the EEPROM based on the configuration size of the data that you are intending to store in the EEPROM. Table 1 describes the EEPROM density for each family of Atmel FPGA and FPSLIC devices.

**Table 1.** EEPROM Density for Atmel FPGA and FPSLIC Devices

| FPGA/FPSLIC | Memory Required | Configurator | Configurator Size |
|---|---|---|---|
| AT94K05AL | 226,520 bits | AT17LV256 | 256K = 262,144 bits |
| AT94K10AL | 430,488 bits | AT17LV512 | 512K = 524,288 bits |
| AT94K40AL | 815,382 bits | AT17LV010 | 1M = 1,048,576 bits |
| ATK40K05/LV/AL | 42,104 bits | AT17LV65 | 65K = 66,560 bits |
| AT40K10/LV/AL | 89,400 bits | AT17LV128 | 128K = 131,072 bits |
| AT40K20/LV/AL | 154,232 bits | AT17LV256 | 256K = 262,144 bits |
| AT40K40/LV/AL | 336,504 bits | AT17LV512 | 512K = 524,288 bits |

To find out which Xilinx® or Altera® EPROM can be crossed to Atmel AT17LV series EEPROM search Atmel Configurators Cross-Reference database on the Atmel web site, at http://www.atmel.com/atmel/products/xref22.shtml.

For microprocessor chips, observe the size of the bit-stream file in order to select the correct parts of EEPROM.

## AT17LVxxx and AT17LVxxxA Configurators

Atmel AT17LV series EEPROMs are available in two versions: AT17LVxxx - pin compatible with Xilinx EEPROMs - and a AT17LVxxxA - pin compatible with Altera EEPROMs.

Only the high-density configurators, AT17LV512(A)/010(A)/020(A)/002(A)/040, have internal oscillators. The internal oscillator of the AT17LV512A/010A/020A/002A EEPROM is enabled by default, but is disabled for the AT17LV512/010/020/002/040 EEPROMs, see Table 2.

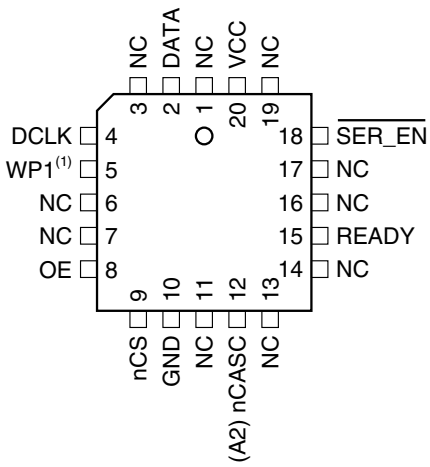
**Table 2.** “A” and “Non-A” Part EEPROMs

| AT17LV65A/128A/256A | AT17LV65/128/256 |
|---|---|
| No internal oscillator | No internal oscillator |
| “A” parts are recommended for Altera users | “Non-A” parts for all other applications |
| 20-pin PLCC Altera pinout | 20-pin PLCC Xilinx pinout |
| **AT17LV512A/010A/020A/002A** | **AT17LV512/010/020/002/040** |
| Internal oscillator is enabled by default(1) | Internal oscillator is disabled by default |
| “A” parts are recommended for Altera users | “Non-A” parts for all other applications |
| 20-pin PLCC Altera pinout | 20-pin PLCC Xilinx pinout |
| 8-pin PDIP/LAP, same pinout with oscillator enabled | 8-pin PDIP, same pinout with oscillator disabled |

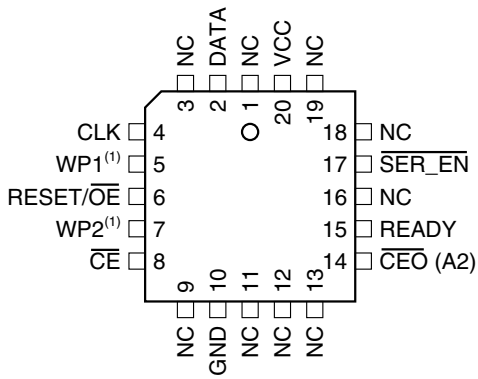
Note: 1. Oscillator must be enabled to program Altera’s FLEX® 20K, 10K, 6K and 1K. It must be disabled to program Altera’s FLEX 8K

**Figure 1.** "A" Part and "Non-A" Part Pinouts

**20-pin PLCC "A" Part**




**20-pin PLCC "Non-A" Part**




Note: 1. AT17LV020 and AT17LV020A do not have a write protect pin (WP1 or WP2).

## Selecting the Package Type

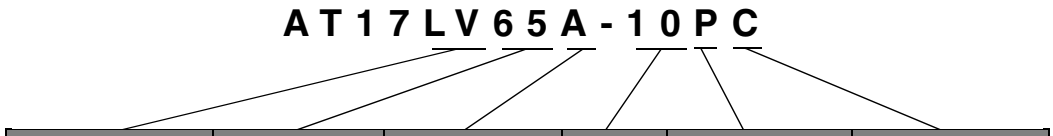
**Table 3.** Package Availability

| AT17LVxxx | 8-pin PDIP | 8-pin SOIC | 8-pin LAP | 20-pin PLCC | 20-pin SOIC | 44-pin PLCC | 44-pin TQFP |
|---|---|---|---|---|---|---|---|
| AT17LV65 | x | x | x | x | x | | |
| AT17LV128 | x | x | x | x | x | | |
| AT17LV256 | x | x | x | x | x | | |
| AT17LV512 | x | | x | x | | | |
| AT17LV010 | x | | x | x | | | |
| AT17LV020 | | | | x | | | |
| AT17LV002 | | | x | x | | x | x |
| AT17LV040 | | | | | | x | x |

| AT17LVxxxA | 8-pin PDIP | 20-pin PLCC | 32-pin TQFP |
|---|---|---|---|
| AT17LV65A | x | x | |
| AT17LV128A | x | x | |
| AT17LV256 | x | x | |
| AT17LV512 | x | x | |
| AT17LV010 | x | x | |
| AT17LV020 | | x | |
| AT17LV002 | | x | x |

## Determining the Ordering Code

**Figure 2.** Ordering Code




| Voltage | Density | Pinouts | Speed | Package | Temperature |
|---|---|---|---|---|---|
| LV = 3.3V and 5V | 65 = 64K<br>128 = 128K<br>256 = 256K<br>512 = 512K<br>010 = 1M<br>020 = 2M(1)<br>002 = 2M(2)<br>040 = 4M | A = Altera<br>Blank = Xilinx/ Atmel | 10 | C = 8LAP<br>P = 8 PDIP<br>N = 8 SOIC<br>J = 20 PLCC<br>S = 20 SOIC<br>Q = 32 TQFP<br>BJ = 44 PLCC<br>TQ = 44 TQFP | C = Commercial<br>I = Industrial |

Notes: 1. Multiple Chip Module
2. Monolithic Chip Module

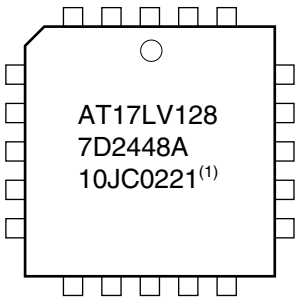
**Table 4.** Package Description

| Package | Description |
|---|---|
| 8 LAP | 8-lead, 6 mm x 6 mm, Leadless Array Package (LAP) |
| 8 PDIP | 8-pin, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| 8 SOIC | 8-lead, 0.150" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC) |
| 20 PLCC | 20-lead, Plastic J-leaded Chip Carrier (PLCC) |
| 20 SOIC | 20-lead, 0.300" Wide, Plastic Gull Wing Small Outline (JEDEC SOIC) |
| 32 TQFP | 32-lead, Thin Plastic Quad Flat Package Carrier (TQFP) |
| 44 TQFP | 44-lead, Thin (1.0 mm) Plastic Quad Flat Package Carrier (TQFP) |
| 44 PLCC | 44-lead, Plastic J-leaded Chip Carrier (PLCC) |

## Reading the Device Markings

An example of the device marking is described in Figure 3. The first line specifies the name and the density of the EEPROM. The second line defines the lot code of the device. The third line provides information about the package type and the date code of the original chip from assembly.

**Figure 3.** Device Label




Device Name and Density: AT17LV128
Lot Code: 7D2448A
Package Type: 10JC
Date Code: 0221(1)

Note: 1. Week 21 of 2002.

## Programming Options

Atmel AT17LV series EEPROMs are supported by Atmel ATDH2200E Programming Kit, the ATDH2225 ISP cable and many third-party programmers such as DATA/IO, BP, Hi-Lo, Logical Devices, Dataman, etc.

The “AT17LV series FPGA Configuration EEPROM Programmer Status” application note, available on the Atmel web site (www.atmel.com) provides information on the third-party programmers that support Atmel AT17LV series. For the latest update on the device support, please visit the web site of the third-party programmer.

There are two ways to program Atmel AT17LV series EEPROMs:

- Drop-In/Standalone Programming. The configurator is first programmed and then dropped into a circuit to program the FPGA, the FPSLIC or the microcontroller.
- In-System Programming (ISP). The configurator is soldered on the target board and connected to the FPGA, the FPSLIC or the microcontroller through a programming cable.

The complete programming circuits can be downloaded from the Configuration Memories section of the Atmel web site.

## Programming File Formats

Both the ATDH2200E programming kit and the ATDH2225 ISP cable use Atmel’s Configurator Programming System (CPS) software to program the EEPROM. CPS accepts Atmel’s binary (*.bst) file, Xilinx’s (*.mcs) file, Intel’s (*.hex) file, and Altera’s (*.pof) and (*.rbf) files. For more details, please refer to the CPS user manual.

To program Atmel’s EEPROMs with a third-party programmer, check the user manual of the programmer to see what kind of file format can be imported. Most third-party programmers accept Intel®’s MCS®86 hex object file format (*.hex) or (*.mcs).

To program Atmel’s EEPROMs for an AT40K FPGA using a third-party programmer, use the (*.hxr) file - the reversed hex object file that is generated by Atmel’s Place and Route tool, IDS. This file can also be renamed to (*.hex) and used as Intel’s MCS86 hex object file when using with a third-party programmer.

## Troubleshooting Hints

If there is an error message reported by CPS software, compare your software and hardware settings with those provided by the user manual or the online Troubleshooting Guide.

If the problem still cannot be solved, contact the configurator support hotline at +1(408)436-4119 (USA) or e-mail the log file (cps.lst) to configurator@atmel.com.

If using a third-party programmer the reset polarity option in the programmer might not have been set correctly. If the reset polarity is programmed to be Low ($\overline{\text{RESET}}$/OE), it will require a High signal to enable OE. If the reset polarity is programmed to be High (RESET/$\overline{\text{OE}}$), it will require a Low signal to enable $\overline{\text{OE}}$. The OE pin is used as a control signal to enable the output tri-state data buffer of the EEPROM. The reset polarity by default is High.

When using Atmel's CPS software with the ATDH2200 programming boards, the reset polarity programming option can be easily selected from the software window. However, to set the RESET polarity level of the EEPROM using a third-party programmer such as DATA/IO Unitsite programmer, you need to edit some bits from the Ram buffer of the programmer after the file is imported.

Table 5 shows the reset polarity level for the Data I/O programmer.

**Table 5.** Device Address Location Data

| Device | reset Low | reset High |
|---|---|---|
| AT17LV65 | 2000-2003 00h | 2000-2003 FFh |
| AT17LV128 | 4000-4003 00h | 4000-4003 FFh |
| AT17LV256 | 8000-8003 00h | 8000-8003 FFh |
| AT17LV512 | 10000-10003 FFh | 10000-10003 00h |
| AT17LV010 | 20000-20003 FFh | 20000-20003 00h |
| AT17LV020/17LV002 | 40000-40003 FFh | 40000-40003 00h |
| AT17LV040 | 80000-80003 FFh | 80000-80003 00h |

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